IN THE CLAIMS

Rewrite the pending elected claims as follows:

1. (Currently Amended) A memory system comprising:

a memory controller connected to at least one channel;

memory devices connected to the at least one channel, wherein at least one of the memory devices is a low bandwidth device being individually incapable of communicating a first data block with the memory controller during a first time period;

wherein the memory controller is configured to communicate control information to at least a first plurality of the memory devices via the at least one channel, and the first plurality of memory devices, as a multiplexed group on the channel, are configured to communicate a first data block between the memory controller and the first plurality of the memory devices during a the first time period in response to the control information.

2. (Original) The memory system of claim 1, wherein each one of the first plurality of memory devices is configured to contribute a second data block, less than the first data block, to the first data block communicated during the first time period.

3. (Original) The memory system of claim 2, wherein the at least one channel comprises two channels, each one of the two channels connecting a second plurality of memory devices to the memory controller.

4. (Original) The memory system of claim 3 wherein the second plurality of memory devices comprises sixteen memory devices.

5. (Original) The memory system of claim 2, wherein the at least one channel comprises four full channels and one half channel, each one of the full channels connecting a second plurality of memory devices, and the one half channel connecting half the second plurality of memory devices.

6. (Original) The memory system of claim 5, wherein the second plurality of memory devices comprises sixteen memory devices.

7. (Original) The memory system of claim 2, wherein the at least one channel comprises eight channels, each channel connecting a second plurality of memory devices.

8. (Original) The memory system of claim 7, wherein the second plurality of memory devices comprises eight memory devices.

9. (Original) The memory system of claim 2, wherein the at least one channel comprises four channels, each channel connecting a second plurality of memory devices.

10. (Original) The memory system of claim 9, wherein the second plurality of memory devices comprises eight memory devices.

11. (Currently Amended) A memory system comprising:

a memory controller connected to at least one repeater via a main channel;

wherein each repeater connects a first plurality of memory devices via at least one auxiliary channel, and wherein each one of the first plurality of memory devices is a low bandwidth device individually incapable of communicating a first data block with the memory controller during a first time period;

wherein the memory controller is configured to communicate control information to the first plurality of the memory devices via the at least the main channel, the at least one repeater, and the at least one auxiliary channel, and the first plurality of memory devices, as a multiplexed group on the channel, are configured to communicate a first data block between the memory controller and the first plurality of the memory devices during a the first time period in response to the control information.

12. (Original) The memory system of claim 11, wherein each memory device in the first plurality of memory devices contributes a second data block, less than the first data block, to the first data block transferred during the first time period.

13. (Original) The memory system of claim 11, wherein the at least one repeater connects a second plurality of memory devices via a first auxiliary channel, and connects a third plurality of memory devices via a second auxiliary channel.

14. (Original) The memory system of claim 13, wherein each one of the second and third pluralities of memory devices comprises eight memory devices.